REMARKS

Status Summary

Claims 1-8 and 10-16 are pending in the present application, all of which presently stand rejected.

Specification

The Examiner has stated that the guidelines laid out in 37 CFR 1.77(b) illustrate the preferred layout for the specification of a utility application. Applicant again respectfully directs the Examiner's attention to the Preliminary Amendment filed with the present application on July 8, 2003. Within that Amendment, Applicant inserted within the specification appropriate section headings. To the extent that the amendments outlined in that Preliminary Amendment have not been made part of the application, it is requested that relevant section headings be inserted as indicated by the amendments above, which are repeated from the Preliminary Amendment. Therefore, Applicant respectfully submits that the objections to the specification should be withdrawn.

Claim Rejection - 35 U.S.C. § 103

Claims 1-7 and 10-16 stand rejected by the Examiner under 35 U.S.C. § 103(a) as being unpatentable over Tsui et al. (Low Power ACS Unit Design for the Viterbi Decoder: May 30, 1999 IEEE International Symposium on Circuits and Systems, page 137-140.) (hereinafter, "Tsui") in view of U.S. Patent No. 5,341,387 to Nguyen et al. (hereinafter, "Nguyen") and further in view of U.S. Patent No. 5,371,471 to Chennakeshu et al. (hereinafter, "Chennakeshu") and U.S. Patent No. 5,991,341 to

Shin (hereinafter, "Shin"). Claim 8 stands rejected under 35 U.S.C. § 103(a) as being unpatentable over Tsui in view of Nguyen and further in view of Chennakeshu, Shin, and U.S. Patent No. 4,879,729 to Salembier et al. (hereinafter, "Salembier"). Specifically, the Examiner contends that Tsui discloses the features of elements (a) and (b) of claim 1. With respect to feature (c) of claim 1, the Examiner contends that Nguyen describes a selection circuit which temporarily stores only those path metrics whose validity value is logic high in a memory. With respect to feature (d) of claim 1, the Examiner further contends that Shin discloses two or more logic validity values which are produced by the path metric calculation circuit are logically OR-linked by a logic circuit. Finally, with respect to claim 8, which depends from claim 1, the Examiner contends that Salembier discloses a power value to the base two. The positions of the Examiner as summarized above with respect to claims 1-8 and 10-16 are respectfully traversed as described below.

With respect to element (c) of claim 1, Nguyen teaches the decision state machine or decision circuit **130** is provided with the comparison results of the comparator **120** (Figures 9, 11). The comparator **120** compares a threshold value and a sum which is generated by an adder **116** by combining a data sample from the data sample input with a delayed data sample. Even if it is assumed that the sum generated by the adder **116** corresponds to the calculated path metrics as defined according to the present claims (i.e., so that logic validity values are provided from the comparator **120** to the state machine **130**), Nguyen teaches that the decision state machine or decision circuit **130** provides output signals **da** and **db**, which are sent into a memory path circuit

134 (Figures 9, 11; col. 12, lines 25-27 and 53-56). Particularly, the output signals **da** and **db** are always sent and stored in the memory path circuit **134**. Applicant respectfully asserts that Nguyen fails to teach or suggest that only a selection of the calculated path metrics (i.e., those path metrics whose logic validity value is high) is temporarily stored in a memory.

In addition, the output signals **da** and **db** which are stored in the memory path circuit **134** do not correspond to path metrics as defined according to the present claims. According to the present claims, the path metrics are compared with the decision threshold value, and additionally they are temporarily stored in a memory if the result of the comparison leads to a logic high validity value. In contrast, even if it is again assumed that the sum generated by the adder **116** disclosed by Nguyen corresponds to a path metric, it is not this sum that is stored in the memory path circuit **134**. Rather, it is the output signals **da** and **db** of the decision state machine **130** that are stored in the memory path circuit **134**. These output signals **da** and **db** are different than the sum that, for the sake of this argument, corresponds to a path metric.

With respect to element (d) of claim 1, Shin teaches the OR-gate **434** is part of a normalizer **430** (Figure 13; col. 16, lines 33-35). The normalizer **430** is used for preventing an overflow since the path metrics are limited to twelve bits, respectively. Therefore the normalizer **430** checks the MSB of each of the new path metrics **new_pm0** through **new_pm7**. If any of the MSBs are equal to "1", all path metrics are shifted to the right by one bit, thereby outputting normalized path metrics **no_out0** through **no_out7** (Col. 13, line 64 – col. 14, line 5). The OR-gate **434** thus OR-links the

MSBs of the new path metrics **new_pm0** through **new_pm7** to check whether the path metrics have to be normalized. It is respectfully submitted that the function and connection of the OR-gate **434** are different than the OR-linking according to the present claims.

According to the present claims, it is the validity values that are OR-linked. The validity values are results of the comparisons of the path metrics and the threshold value. Applicant respectfully disagrees with the Examiner's interpretation that the MSBs of the new path metrics **new_pm0** through **new_pm7** according to Shin correspond to the validity values according to the present claims.

In addition, the Examiner cites Nguyen to show the validity values are stored in the selection circuit. There does not exist a basis, however, for the person skilled in the art to integrate the OR-linking as disclosed in Shin to OR-link the validity values of Nguyen. Because it is asserted that the MSBs of the new path metrics **new_pm0** through **new_pm7** according to Shin do not correspond to the validity values according to the present claims, it is submitted that the person skilled in the art would not incorporate the OR-linking as disclosed by Shin within the teaching of Nguyen to OR-link the comparison results of the comparator **120** of Nguyen that are regarded to be the validity values.

Further, even if it might have been possible for the person skilled in the art to incorporate the OR-gate **434** within the system of Tsui, the Examiner recognizes that the person skilled in the art would only have done this to realize a normalization to prevent an overflow. As such, this combination of references would still not have led

the person skilled in the art to the arrangement as claimed because such normalization is not the function of the OR-linking according to the present claims. The OR-linking according the present claims is incorporated so that the selection circuit stores a total decision vector, which comprises N_{PE} decision values, in the integrated memory. It is thus further submitted that the person skilled in the art would not look to the OR-gate **434** taught by Shin to OR-link two or more logic validity values as is disclosed by the present claims.

Accordingly, features (c) and (d) of claim 1 are neither taught nor suggested by Tsui, Nguyen, Chennakeshu, and Shin, either alone or in combination, and it is respectfully submitted that claims 1-7 and 10-16 are thus in proper condition for allowance.

With respect to the separate rejection of claim 8, Nguyen does teach programmable threshold levels on lines **100** and **102**. As noted above, however, Nguyen fails to teach or suggest that only a selection of the calculated path metrics is temporarily stored in a memory, as is recited in element (c) of claim 1 from which claim 8 depends. Further, Shin fails to teach or suggest two or more logic validity values being OR-linked as is recited in element (d) of claim 1. The addition of Salembier to teach active coefficients having a power of two within a filter does not overcome the deficiencies of Nguyen and Shin.

In addition, the coefficients having a power of two taught by Salembier are not used as threshold values for comparison with calculated path metrics. Rather, the coefficients are used for shifting bits of successive samples $X_{k\pm l}$ that are representative

of a digital transmitted signal (Col. 4, line 62 – col. 5, line 22). It is thus submitted that a person having skill in the art would not look to Salembier to provide that the adjustable decision threshold value is a power value to the base two as is disclosed by claim 8. Accordingly, it is further respectfully submitted that Tsui, Nguyen, Chennakeshu, Shin, and Salembier, either alone or in combination, fail to teach or suggest every element of claim 8, and claim 8 is thus in proper condition for allowance.

CONCLUSION

In light of the above amendments and remarks, it is respectfully submitted that the present application is now in proper condition for allowance, and an early notice to such effect is earnestly solicited.

If any small matter should remain outstanding after the Patent Examiner has had an opportunity to review the above Remarks, the Patent Examiner is respectfully requested to telephone the undersigned patent attorney in order to resolve these matters and avoid the issuance of another Official Action.

DEPOSIT ACCOUNT

The Commissioner is hereby authorized to charge any fees associated with the filing of this correspondence to Deposit Account No. **50-0426**.

Respectfully submitted,

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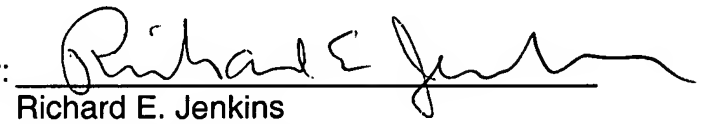
Date: August 9, 2007

By: 
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